Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Fourth Semester B.Tech Degree Examination July 2021 (2019 Scheme)

Course Code:CST202

Course Name: Computer Organization and Architecture

Max. Marks: 100 Duration: 3 Hours

PART A

(Answer all questions; each question carries 3 marks) Marks

1		Compare auto increment and auto decrement addressing modes with examples	3
2		Outline the steps involved in the execution of an instruction.	3
3		How is the two port memory organization of processor unit better when compared to scratch pad memory organization?	3
4		Give the block diagram of circuit that implements following statements in register transfer logic: T_1; C ←A T_5: C ←B	3
5		Draw the flow chart for Booth's Multiplication Algorithm	3
6		Illustrate Read After Write (RAW) hazard with an example	3
7		Explain PLA based control organization with the help of a diagram	3
8		Differentiate between horizontal and vertical microinstructions	3
9		List and explain the different types of ROMs	3
10		Explain the term locality of reference. How is this related to cache memory?	3

PART B

(Answer one full question from each module, each question carries 14 marks)

Module -1

11	a)	Identify the addressing modes that can be used for representing the following higher level language constructs in machine level. Illustrate each addressing mode using an example. 1) Arrays 2) Pointers 3) Constants 4) Variables	4

b) Illustrate the single bus organization of processor unit with the help of suitable diagrams. Explain, listing the control signals, how the following operations are handled in this organization. 10

i) Transfer contents of register R5 to R1

ii) Move (R6), R2 (*Fetch a word from memory and move it to register R2, when the memory address is stored in register R6*)

OR

12 a) Outline the differences in instruction execution during straight line sequencing and branching using suitable examples. 7

b) Differentiate between big endian and little endian byte ordering. 7

Consider a computer that has a byte addressable memory organized as 32 bit words. A program reads ASCII characters entered at a key board and stores them in successive byte locations, starting at location 1000. Show the contents of the two memory words at locations 1000 and 1004 after the name *Johnson* has been entered in case:

i) Big Endian Byte ordering is used

ii) Little Endian Byte ordering is used

(ASCII equivalent of characters in *Johnson* in hex will be 4A, 6F, 68, 6E, 73,6F, 6E. You can indicate unused byte locations using XX).

Module -2

13 a) Illustrate and explain the organization of a processor unit where processor registers and ALU are connected through common buses. Explain how the micro operation **R2 ← R3+R4** would be performed using this organization, where R2, R3 and R4 are processor registers. 7

b) Explain with the help of a block diagram the design of a 4 bit status register for an 8 bit ALU. The four status bits are C (carry), S(sign), Z(zero) and V (overflow). Clearly indicate the purpose of each status bit and how they are set or reset. 7

OR

14 a) Design and draw a combinational logic shifter using multiplexers with two selection variables, H_1 and H_0. The operations of shifter should be as specified in the following table: 10

H_1	H_0	Operation	Function
0	0	S←0	Transfer 0's to S
0	1	S←shl F	Shift left F into S
1	0	S←shr F	Shift right F into S
1	1	S←F	No shift

b) Describe about arithmetic, logic and shift micro operations, listing the available operations in each category. 4

Module -3

15 a) Outline the hardware requirement for multiplying two binary numbers in sign magnitude format and specify a flowchart for same. Illustrate the algorithm, showing the contents of registers, for the multiplication of **11111** by **10101** 8

b) Explain the various pipeline structures available inside a computer 6

OR

16 a) Design and draw the block diagram for a 4 by 3 array multiplier. 8

b) Explain the various method available to get rid of data hazards inside the system 6

Module -4

17 a) Illustrate the working of a micro program sequencer with the help of diagrams 7

b) Outline with the help of a block diagram, how a micro program control unit can be used for controlling the processor unit. 7

OR

18 Illustrate the steps for designing a micro programmed control circuit for the addition and subtraction of binary numbers in sign magnitude form. Specify the block diagram of control circuitry and the binary micro program for control memory. 14

Module -5

19 a) Explain with examples the three types of mapping functions used in cache memory 7

b) What are interrupts? Outline the actions taking place in a processor once an interrupt has been raised. 7

OR

20 a) What is a DRAM? Compare the two types of DRAMs, highlighting their differences. 7

b) Outline how Direct Memory Access is implemented? Differentiate between cycle stealing DMA and burst mode DMA. 7

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